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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,563	07/24/2003	Shigeo Kigo	P23980	8106

7055 7590 09/21/2005

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EXAMINER	
WU, XIAO MIN	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,563	KIGO ET AL.	
	Examiner	Art Unit	
	XIAO M. WU	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/868,660.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3-8-04, 9-28-04, 9-20-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-6, 10-12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by 102(b) Turney (US Patent No. 4,495,445).

As to claims 1, 12, Turney discloses a driving circuit (Fig. 1) that drives a display panel (14) having an electrode (12, 13), comprising: a transistor (52) connected to a power supply (16, 18, 19); an interconnector (25) connected to said transistor; and a frequency reducer (54, Fig. 1, also see col. 8, lines 32-37) connected in parallel with a source and a drain of said transistor, wherein a potential of the power supply (19) is applied to the electrode (12, 13) of the display panel (14) through said transistor (52) and said interconnector (25).

As to claims 4. 14, Turney discloses a driving circuit (Fig. 1) that drives a display panel (14) having an electrode (12, 13), comprising: a transistor (52) connected to a power supply (16, 18, 19); an interconnector (25) connected to said transistor (52); and a frequency reducer having a capacitive element (54, Fig. 1, also see col. 8, lines 32-37) connected in parallel with a source and a drain of said transistor, wherein a potential of the power supply (19) is applied to the electrode of the display panel through said transistor (52) and said interconnector (25).

As to claim 5, Turney discloses a driving circuit that drives (Fig. 1) a display panel (14) having an electrode (12, 13), comprising: a transistor (52) connected to a power supply (16, 18,

19); a first interconnector (25) connected to said transistor (52); a diode (36, 38, 40, 42) connected to said power supply (28, 18, 19); a second interconnector (A, B) connected to said diode and said first interconnector portion (e.g. transformer 16, 28, 18); and a frequency reducer (54) connected in parallel with the said diode (36, 38, 40, 42), wherein the electrode of the display panel is limited to a potential level that does not exceed a potential of the power supply through said diode and said second interconnector (e.g. elements 34 and 39 controlling the voltage applied to the display, see col. 7, lines 11-64).

As to claim 6, Turney discloses a driving circuit that drives a display panel (14) having an electrode (12, 13), comprising: a transistor (52) connected to a power supply (16, 18, 19); a first interconnector (25) connected to said transistor (52); a diode (36, 38, 40, 42) connected to the power supply (28, 18, 19); a second interconnector (A, B) connected to said diode (36, 38, 40, 42) and said first interconnector (e.g. transformer 16, 18, 19); and a frequency reducer (52) having a capacitive element (54) connected in parallel with said diode (36, 38, 40, 42), wherein the electrode of the display panel is limited to a potential level that does not exceed a potential of the power supply through said diode and said second interconnector (e.g. elements 34 and 39 controlling the voltage applied to the display, see col. 7, lines 11-64).

As to claim 10, Turney discloses a driving circuit (Fig. 1) that drives a display panel (14) having an electrode (12, 13), comprising: a transistor (52) connected to a ground; a first interconnector (25) connected to said transistor; a diode (36, 38, 40, 42) connected to said ground; a second interconnector (A, B) connected to said diode (36, 38, 40, 42) and said first interconnector (e.g. 25 is connected to transformer 16, 18, 19) ; and a frequency reducer (54) connected in parallel with said diode (36, 38, 40, 42), wherein the electrode of the display panel

is brought to a potential level that does not exceed a ground potential through said transistor and said second interconnector (e.g. elements 34 and 39 controlling the voltage applied to the display, see col. 7, lines 11-64).

As to claim 11, Turney discloses a driving circuit (Fig. 1) that drives a display panel (14) having an electrode (12, 13), comprising: a transistor (52) connected to a ground; a first interconnector (25) connected to said transistor (52); a diode (36, 38, 40, 42) connected to said ground; a second interconnector (A, B) connected to said diode and said first interconnector; and a frequency reducer having a capacitive element (54) connected in parallel with said diode, wherein the electrode of the display panel is brought to a potential level that does not exceed a ground potential through said transistor and said second interconnector (e.g. elements 34 and 39 controlling the voltage applied to the display, see col. 7, lines 11-64).

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-16 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 6,633,285. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are claiming similar subject mater as illustrated below.

Claim 9 of the instant application is one of representative claim among all the independent claim and is compared with claim 1 of the US Patent 6,633,285 in the following.

Claim 1 of US Patent 6,633,285)	Claim 9 of the instant application
A driving circuit outputting driving pulse to drive a capacitive load, comprising:	A driving circuit that drives a display panel having an electrode, comprising:
an electrical circuit connected to a pulse supply path for supplying said driving pulse to said capacitive load; an interconnection portion connected to said electrical circuit; and	a transistor connected to a ground; an interconnector connected to said transistor; and
frequency reducing circuit for reducing the resonance frequency of LC resonance by the parasitic capacitance of said electrical circuit and inductance component of said interconnection portion.	a frequency reducer having a capacitive element connected in parallel with a source and a drain of said transistor that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of said transistor and an inductance

	component of said interconnector, wherein the electrode of the display panel is brought to a ground potential through said transistor and said interconnector.

From the comparison above, it is noted that claim 9 does not required outputting driving pulse to drive a capacitive load. However, it is well known in the art to have used pulse driving method for driving the display element.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAO M. WU whose telephone number is 571-272-7761. The examiner can normally be reached on 6:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, PATRICK EDOUARD, can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

x.w.

September 19, 2005

XIAO M. WU
Primary Examiner
Art Unit 2674